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GaN-based high output voltage binary and ternary digital components achieved by neutral beam etching

Yudong Li [1], Han Gao [1], Xuanling Zhou, Xinbo Zou [*]

School of Information Science and Technology, ShanghaiTech University, Shanghai 201210, People's Republic of China

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High-performance GaN-based binary and ternary digital modules, including inverter, AND, OR, NAND, and NOR, are demonstrated by integrating D/E-mode GaN MOSHEMTs on a AlGaN/GaN epi-platform, via argon-based neutral beam etching (NBE). Improvement in output voltage swing and transition voltage performance was achieved by optimization of the D/E-mode transistor aspect ratio (W/L). Inverter fabricated with the NBE method yields near unit logic voltage swing of 5.98 V with V_{DD} of 6 V. Balanced low/high-level noise margin of 2.5 V/2.7 V and the transition voltage width of 0.8 V have been obtained. With increasing supply voltage to 8 V, the circuit maintains functional integrity while exhibiting robust performance metrics, including logic voltage swing characteristics of 7.95 V/8 V. In addition, other binary logic components, namely AND, OR, NAND and NOR, all exhibit high voltage swing of over 97%. Furthermore, ternary inverter and NAND modules have been well implemented by integrating multiple E-mode transistors of two different threshold voltages. The output of three logic levels were well documented, showing their great potential in enhancing digital processing capability, facilitating next-generation all-GaN monolithic integration and driving capability.

1. Introduction

Gallium nitride (GaN) high electron mobility transistors (HEMTs) exhibit superior properties under high-voltage and high-frequency conditions, owing to their wide bandgap, high carrier mobility, and low on-resistance (R_{on}), enabling their widespread adoption in power conversion systems [1–3].

Compared with the peripheral circuits (control, drive, and protection circuits) composed of silicon, the monolithic integration of GaN based peripheral circuits and power devices not only improves integration density [4–6] but also minimizes parasitic coupling effects caused by interconnection [7,8]. For example, monolithic integration of digital components with power devices not only enables the implementation of control functions and unleash the high-temperature and high-frequency potential of GaN devices, but also provides the driving capability needed for the power devices [9,10].

The direct-coupled FET logic (DCFL) architecture has been demonstrated to be a feasible method to form essential logic components by integrating D/E-mode n-channel devices [11,12]. In this design, the characteristics of the E-mode devices play a critical role in determining overall circuit performance. Typically, E-mode devices could be realized by p-GaN gate [13–16] and recessed-gate [17–20]; and in recent years, Tri-gate [21] and charge trapping layer [22,23] have also demonstrated good V_{th} modulation.

DCFL circuits with p-GaN gated HEMT are typically confined to low gate voltage operation, e.g., in the range of 3–5V, and lack the capability to deliver the high output voltage required to drive power devices. This limitation is primarily attributed to the low threshold voltage (V_{th}) of p-GaN gated E-mode HEMT. Moreover, when the logic components fabricated by low V_{th} devices are operated at elevated power supply

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* Corresponding author.
E-mail address: zouxb@shanghaitech.edu.cn (X. Zou).

[1] Contributed equally to this work.

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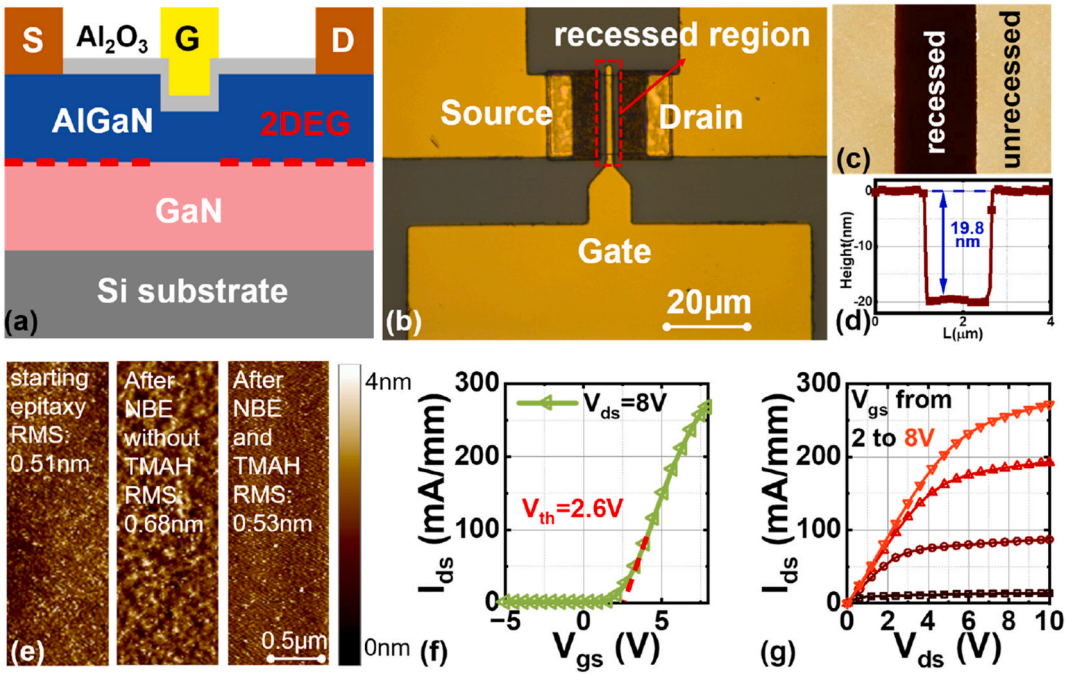

Fig. 1. (a) E-mode device schematic. (b) Optical microscope image of the E-mode device. (c) AFM scanning image and (d) the depth curve of the recess. (e) Characterization of the surface morphology by AFM before NBE (left figure), after NBE without TMAH (middle figure) and after NBE with TMAH (right figure). The (f) transfer and (g) output characteristics of E-mode GaN MOSHEMT.

(V_{DD}) levels, imbalanced noise margins appear, leading to an increase in logical errors caused by cascade circuits.

Recessed-gate devices enable the realization of enhancement-mode operation by modulating the two-dimensional electron gas (2DEG) density through controlled etching of the AlGaN layer thickness beneath the gate, inducing a positive shift in the V_{th} [12,24,25].

In our previous work, the argon-based neutral beam etching (NBE) technique has been employed to form low-damage gate etching and steep sidewall profiles [19]. High-performance recessed gate E-mode GaN transistors have been demonstrated, showing threshold voltage over 4 V and high saturation current simultaneously. The successful demonstration of high-V_{th} HEMT may facilitate meeting the demands of large output voltage and low on-resistance in constructing DCFL.

In the field of digital integrated circuits, fundamental logic gates, such as inverter, AND, OR, NAND, and NOR, serve as essential building blocks. These logic gates not only have a simple structure and are easy to implement, but also can be combined to construct other complex digital functions. This feature simplifies the design and manufacturing process of digital systems and establishes their irreplaceable foundational position in integrated circuits.

Argon-based NBE would enable the fabrication of E-mode devices with various V_{th} by controlling the etch depth of the AlGaN layer beneath the gate, allowing monolithic integration of multiple devices with different V_{th} on a single circuit. For example, multi-value logics can be constructed via integration of several E-mode devices (with various threshold voltages) and D-mode devices, for driver circuits including level shifter, driver control, and dead time control. Previously, monolithic multivalued logic has been proposed to enhance circuit efficiency [26], indicating potential improvements in digital processing density and reduced die area via simulations. Experimental results are yet to be reported.

This work reports high-performance GaN-based binary and ternary digital components by monolithically integrating D/E-mode HEMTs. The fabricated binary digital components, including inverter, AND, OR, NAND, and NOR, exhibit large logic swing, high operating voltage capability, and uniform noise margins. Detailed characterization of basic digital gates validates the robust functionality of these components at an 8 V supply voltage. Furthermore, ternary logic was implemented through interconnecting devices with engineered threshold voltages. The successful demonstration provides preliminary validation of GaN-based multi-valued logic feasibility, laying essential groundwork for its application in expanding digital hierarchies.

2. Device fabrication

As shown in Fig. 1(a), the MOSHEMT were fabricated on AlGaN/GaN epitaxial layer on a silicon substrate. It consisted of a 5 μm AlN/GaN buffer layer, a 210 nm i-GaN channel layer, a 0.8 nm AlN spacer layer, a 23 nm AlGaN barrier layer, and a 2 nm GaN cap layer. Compared to D-mode, E-mode employs a recessed-gate process, in which the AlGaN layer beneath the gate is etched and thinned to enable normally-off operation. The ohmic metal stack composed of Ti/Al/Ni/Au (20/150/50/80 nm) was deposited in source and drain regions, followed by rapid thermal annealing at 790 °C for 40s and 870 °C for 30s. The gate recessing structure was defined by NBE. Featuring a low energy of 200 eV argon beam to minimize damage, nominal AlGaN etching rate of ~3.5 nm/min was achieved for gate recessing. As shown in Fig. 1(c), the AFM image of the recess shows a clear boundary between the etched and unetched parts. Fig. 1(d) showed the trench profile view with a depth of 19.8 nm formed after 5.5 min of etching, verifying the formation of steep sidewalls and good etching morphology. After the NBE processing, the samples were put in preheated 60 °C tetramethylammonium hydroxide (TMAH) for 10 min to further smoothen the surface morphology.

Then, 15 nm-thick Al_2O_3 dielectric layer was deposited immediately by plasma-enhanced atomic layer deposition (PEALD) at 300 °C, which can achieve good density and also serves as a passivation layer for the access regions. Finally, after opening the hole in the oxide layer, gate metal and contact pads were formed by Ni/Au (20/200 nm). Fig. 1(b) showed the optical microscope image of the E-mode device, and the recessed structure was under the gate metal. As shown in Fig. 1(e), the root-mean-square (RMS) roughness of the starting epitaxy was 0.51 nm. After NBE process, the RMS roughness increased to 0.68 nm without significantly affecting the roughness. After NBE process and TMAH treatment the RMS became 0.53 nm, indicating a minimal micro-

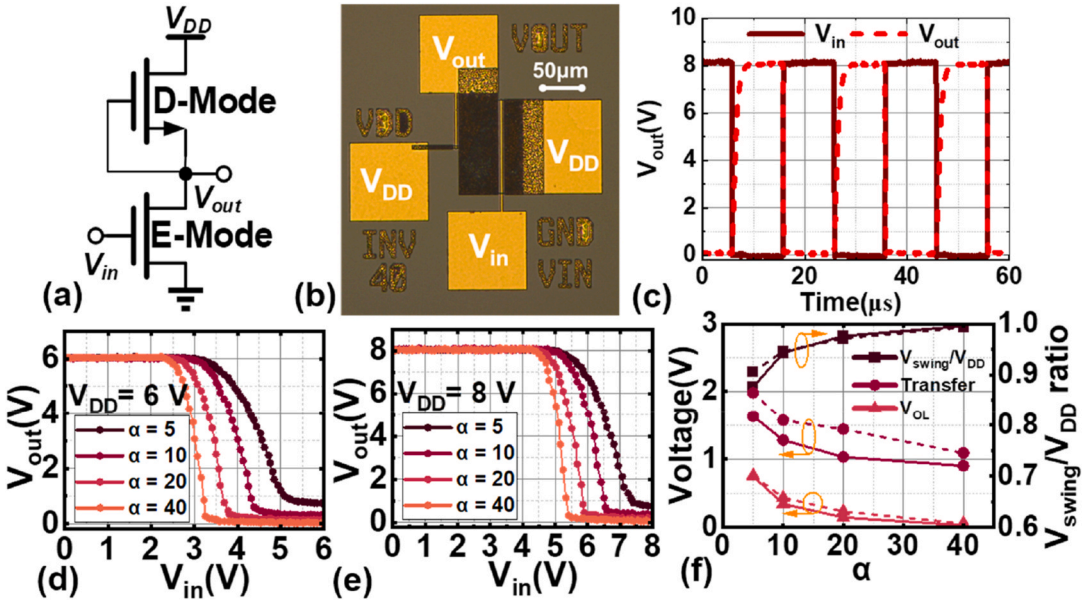

Fig. 2. (a) Schematic of DCFL inverter including a D-mode MOSHEMT and E-mode MOSHEMT. (b) Optical microscope image and (c) input-output waveforms of the fabricated inverter with driver-to-load ratio α = 40. Voltage transfer characteristics of inverters with different driver-to-load ratio α from 5 to 40, with V_{DD} of (d) 6V and (e) 8V, respectively. (f) The impact of increasing α on performance (The solid line denotes results with V_{DD} = 6 V, and the dashed line denotes results with V_{DD} = 8V).

roughness and highly smooth etching surface achieved by NBE. The V_{th} of the device will increase with the increase of etching depth, thus becoming an E-mode device. Fig. 1(f) illustrated the transfer characteristics of the normally-off GaN MOSHEMT with an etching depth of 19.8 nm and a remaining AlGaN thickness of 6.2 nm. The normally-off device exhibited a V_{th} of 2.6 V, which was determined using a linear extrapolation method. The output characteristics of the normally-off GaN MOSHEMT were presented in Fig. 1(g). At V_{gs} = 8 V, the normally-off GaN MOSHEMT presented a maximum drain current of 271.6 mA/mm. The normally-on GaN MOSHEMT, which was fabricated by same process without recess, presented a V_{th} of −3.4 V and a maximum drain current of 275.9 mA/mm at V_{gs} = 0 V. The gate width W_g, gate length L_g, gate-source distance L_{gs}, and gate-drain distance L_{gd} of the D/E-mode GaN MOSHEMTs were 20/1.5/1.5/2 μm, respectively.

3. Digital design and characteristics

3.1. Inverter

As shown in Fig. 2(a), the inverter is formed by directly coupling a D-mode device (configured as the load transistor) and an E-mode device (configured as the drive transistor). Fig. 2(b) showed a typical optical microscope image of the fabricated inverter with α = 40. In this study, inverters with different driver-to-load ratio, which is defined as $\alpha=(W/L)_E/(W/L)_D$, were fabricated. The W is the width of the gate and L is the length of the gate. In DCFL type inverters and under the condition of simultaneous conduction, the circuit can be approximated by a resistive divider network. The output voltage is related to their resistance ratio and can be expressed as $V_{OL} = R_E/(R_D + R_E) \times V_{DD}$. Increasing the value of α can reduce the equivalent resistance of E-mode, thereby lowering the output voltage and improving the performance of the circuit. Compared to the case where the current in D-mode is much larger than that in E-mode, this improvement is more pronounced when the current density in D/E-mode is comparable [27].

Fig. 2(c) presented the voltage transfer characteristics under square-wave input signals. The inverter maintained a correct voltage of a square wave and the high-level output voltage (V_{OH}) and low-level output voltage (V_{OL}) were 8 V and 0.02 V, respectively, yielding a large voltage swing of 7.98 V/8 V (99.75%). Fig. 2(d, e) showed the voltage transfer characteristics of DCFL inverter for the V_{DD} of 6 V and 8 V, respectively. Fig. 2 (f) showed the impact of increasing α on performance. The results

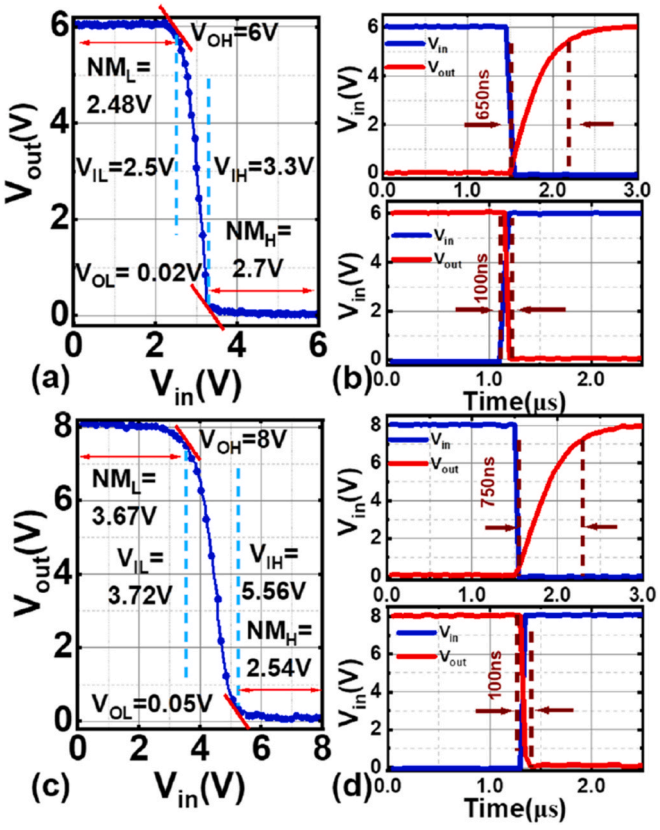

Fig. 3. Voltage transfer characteristic of the inverter with a ratio α of 40 at V_{DD} = 6V (a) and 8V (c). The rise time and fall time of inverter with (b) V_{DD} = 6V and (d) 8V.

Table 1
Comparison of DCFL inverters in the literature.

Affiliation	V_{DD}(V)	V_{swing}(V)	NM_L(V)	NM_H(V)
[15]	5	4.66 (93.2%)	1.58	2.00
[16]	3	2.91 (96.7%)	0.78	1.67
[25]	7	6.30 (90.0%)	2.30	3.10
[31],[a]	3	2.91 (96.7%)	0.20	2.40
[30],[a]	6	5.80 (96.7%)	1.70	2.20
[32]	7/10	6.68 (98%)/9.80 (98%)	2.75/3.44	3.54/4.79
This work	6/8	5.98 (99.7%)/7.95 (99.4%)	2.48/3.67	2.70/2.54

[a] Extracted data from graph.

indicate that with the increase of α, the equivalent resistance of E-mode decreases and the driving capability increases, resulting in lower V_{OL} and higher voltage swing. At the same time, it also reduces the transfer voltage (Defined as the V_{in} range required for the output to change from V_{OH} to V_{OL}) and making the inverter to have sharper transition.

The magnitude of the low output voltage is directly constrained by the performance characteristics of the E-mode transistor. The recessed-gate E-mode transistor fabricated by NBE demonstrated low on-resistance characteristics, enabling significant reduction in low-level output voltage. By increasing the W/L of the E-mode device, the resistance contribution from the E-mode transistor is further minimized and the low-level output voltage can be further reduced, thereby achieving enhanced output voltage swing. Fig. 3(a) showed the corresponding static voltage transfer curve with a supply voltage V_{DD} of 6 V. The V_{OH} and V_{OL} voltages of the inverter are 6 V and 0.02 V, respectively, corresponding to an output voltage swing of 5.98 V/6V (99.7%). The input low (V_{IL}) and high (V_{IH}) voltage levels, extracted from the voltage unit gain points ($dV_{out}/dV_{in} = -1$) are 2.5 V and 3.3 V, respectively. The low-level noise margin ($NM_L = V_{IL}$-V_{OL}) and high-level noise margin ($NM_H = V_{OH}$-V_{IH}) are 2.48 V and 2.7 V, respectively. As shown in Fig. 3(c), the output voltage swing is well-maintained as 7.95 V/8 V (99.38%) when V_{DD} increases to 8V and enhancements are observed in V_{IL} and V_{IH} with measured values of 3.67 V and 5.56 V. Concurrently, a significant improvement in low-level noise margin is observed (increasing from 2.48 V to 3.67 V). This is because the increase in V_{DD} enhances the pull-up capability of D-mode, while E-mode requires a larger gate voltage to provide stronger pull-down capability in order to lower the output level. Therefore the value of V_{IL} and NM_L were improved. Additionally, Fig. 3 (b) and (d) exhibit the rise and fall times (defined as the transition time when the output switches from 10% to 90% of the maximum value) of different V_{DD} at 50 kHz. The rise times are 650 ns and 750 ns, respectively, and the fall times are both 100 ns. Due to the increase in the final required voltage and the electron traps caused by high bias voltage, which cause a slight decrease in current [28,29], the rise time is longer at V_{DD} = 8V than at V_{DD} = 6V. Rise/Fall time demonstrate nanosecond-scale switching capability. Due to the structural characteristics of DCFL, there is a DC path from V_{DD} to GND when the input is high, resulting in a static power consumption of 3.46 mW (Smaller than similar structure in the literature [30], about 8 mW) and an average dynamic power consumption of 1.76 mW when α is 40. Table 1 presents the comparison results of the inverter with those from other literature. These results demonstrate that the inverter fabricated by NBE maintains excellent performance even under high-voltage conditions.

3.2. "And gate" and "OR gate"

As illustrated in Fig. 4(a) and (d), AND and OR gates are implemented using DCFL structures as well. Both utilize a D-mode transistor as the load device, with its gate terminal being directly connected to the

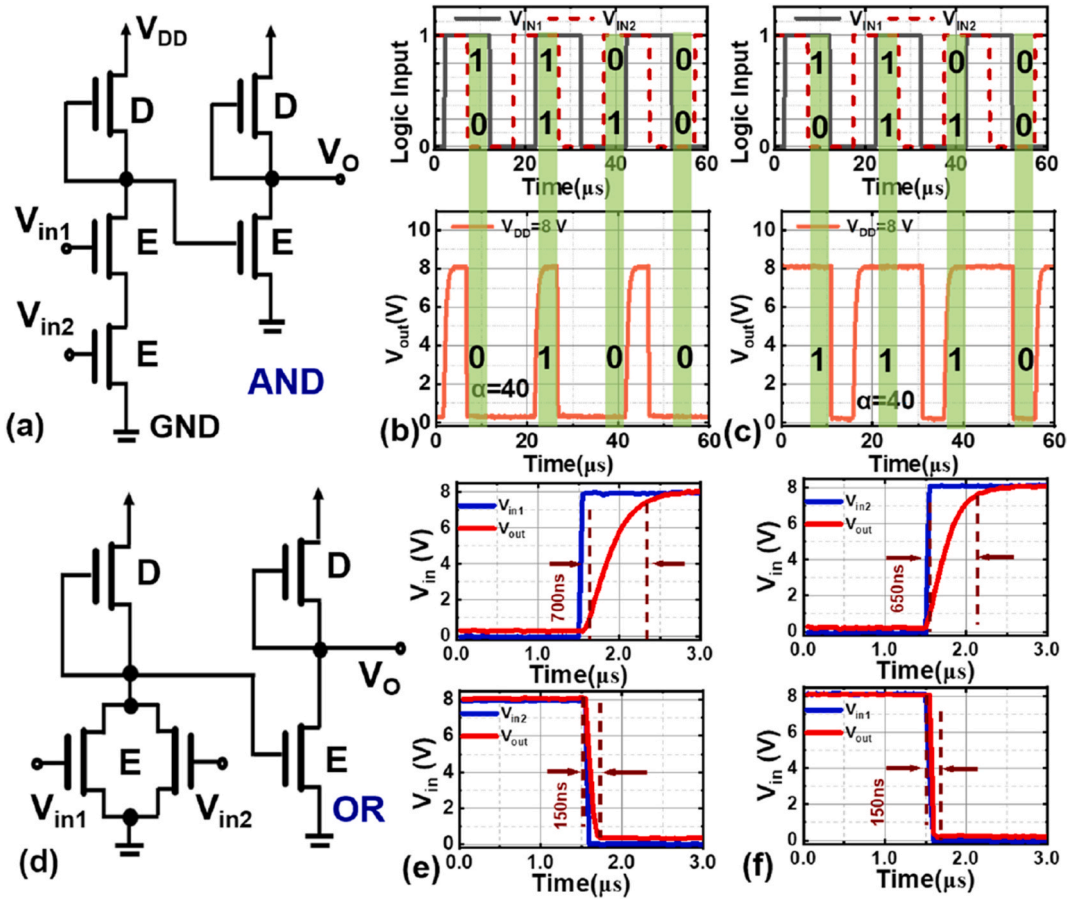

Fig. 4. Schematic of AND (a) and OR (d) circuit, enabled by NBE. Input-output waveform of (b) AND (c) OR at 50 KHz. The rise-fall time of (e) AND and (f) OR.

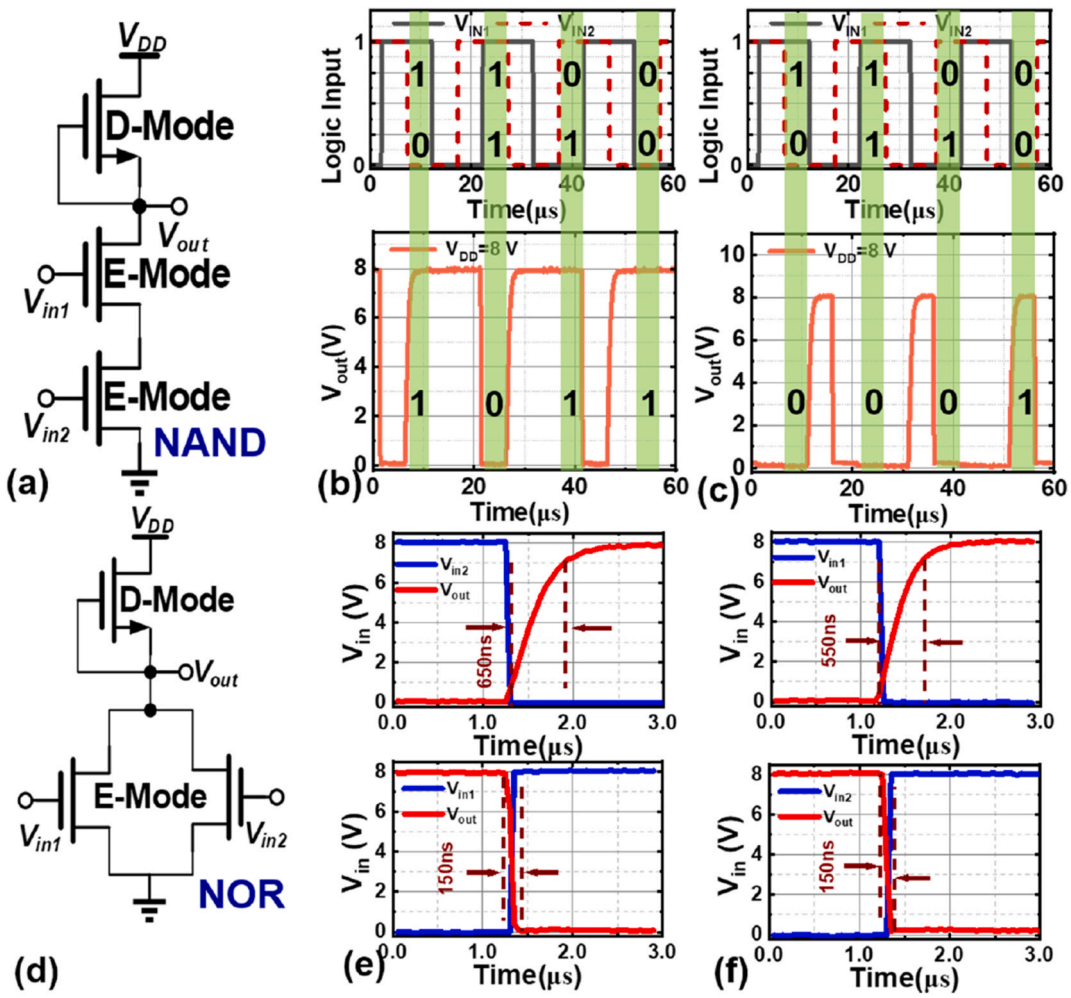

Fig. 5. Schematic of NAND (a) and NOR (d) circuit, enabled by NBE. Input-output waveform of (b) NAND and (c) NOR at 50 KHz. The rise-fall time of (e) NAND and (f) NOR.

output node. The function of the AND gate is achieved through two series-connected E-Mode devices which act as driver transistors. Since the source of E-mode transistors is connected to ground, phase inversion occurs at the output signal. Consequently, an additional inverter—composed of a D-mode and an E-mode transistor—is incorporated at the output stage to ensure correct signal polarity. The input signals V_{in1} and V_{in2} control the two series-connected E-mode transistors to implement the AND logic operation. Furthermore, the performance of the AND gate and OR gate were characterized in Fig. 4(b) and (c) with a V_{DD} of 8V. Input ports V_{in1} and V_{in2} were supplied with square waves phase shifted by 90°, thereby generating the four possible input combinations: 10, 11, 01, and 00. The output characteristic curves of different input signals match the truth table of the AND gate. The AND gate outputs a high level voltage only when both inputs are at high level voltage (11), otherwise, under other input conditions (10, 01, 00) the output remains at a low level voltage. Conversely, the OR gate yields an output at low level voltage only when all inputs are at low level voltage (00); all other input combinations (10, 11, 01) result in a high output. As illustrated by the transfer characteristics, both digital gates maintain correct logical states at elevated V_{DD} and exhibit near-ideal logic voltage swing. As shown in Fig. 4(e) and (f), the measured transfer delay for the AND gate shows rise and fall times of 700ns and 150ns, while those for the OR gate are 650 ns and 150 ns, respectively. From these data, it can be concluded that the average propagation delay of AND and OR is 162.5ns and 100ns, respectively. The larger the capacitance of the device, the longer it takes to charge the node to the corresponding voltage, which deteriorates the time-dependent performance of the circuit.

3.3. "NAND gate" and "NOR gate"

As universal logic gates serving as fundamental building blocks in digital systems, NAND and NOR gates exhibit performance characteristics that critically govern overall system functionality. Consequently, comprehensive characterization of both NAND and NOR gate performance was conducted. As illustrated in Fig. 5(a) and (d), the schematic circuits of NAND and NOR are basically the same as those of AND and OR. However, their structure is simpler and compared to AND and OR, they all lack an inverter. Fig. 5(b) and (c) show the voltage transmission curve (VTC) of the fabricated NAND and NOR logic gates, for which V_{DD} was 8 V, and V_{in1} and V_{in2} were supplied with square waves phase shifted by 90° to be set at 4 different cases. When two input voltage sequences were set as 11, 10, 00, 01, NAND and NOR correctly show output of 0111 and 0010, respectively. The logic voltage swing of NAND (7.98 V/8 V) and NOR (7.95 V/8 V) were both above 99%. Both NAND and NOR gates exhibit favorable transfer speeds, with measured rise/fall times of 650 ns/150 ns for NAND and 550 ns/150 ns for NOR, respectively, as shown in Fig. 5(e) and (f). When the drive transistors are turned off, the output nodes are pulled to a high level by the pull-up current generated by D-mode. The driving transistors of NOR/OR can be equivalent to two finite large resistors in parallel, while the driving transistor of NAND/AND can be equivalent to two finite resistors in series. The overall resistance of NOR/OR is relatively small, and the pull-

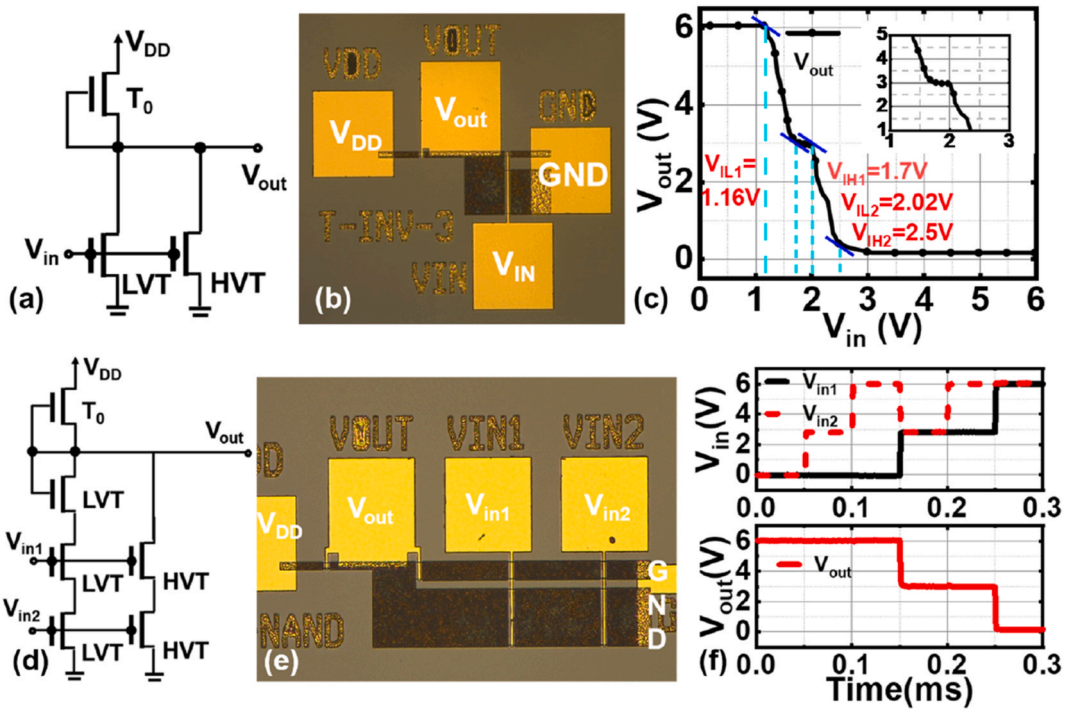

Fig. 6. Schematic diagram of ternary-value (a) inverter and (d) NAND. Optical microscope image of the fabricated (b) ternary inverter and (e)NAND. Output curves of ternary-value (c) inverter which has a median value platform and (f) NAND in different input voltage.

up current generated by D-mode is slightly greater than that in NAND/AND, due to their parallel structure. Therefore, the rise time of NOR/OR is slightly shorter than that of NAND/AND. These results demonstrate the effectiveness of the NBE method in improving the performance of DCFL circuits.

3.4. Ternary logic

For recessed-gate GaN HEMT, the V_{th} is strongly dependent on the recess etching depth. Therefore, monolithic integration of transistors with different V_{th} can be achieved by fabricating devices with different etching depths on the same circuit. As shown in Fig. 6(a), the implementation of the ternary inverter can be achieved through rational design of the V_{th} for E-mode HEMTs (as drive transistors) on different branches and their integration with D-mode HEMT (as load transistor). Fig. 6(b) showed the optical microscope images of the fabricated modules. In constructing a ternary inverter, two types of E-mode devices were utilized, namely low threshold voltage transistor (LVT), which have a recessed gate with 20 nm depth, and high threshold voltage transistor (HVT), which have a recessed gate with 24 nm depth, respectively. When the input voltage exceeds the V_{th} of LVT but remains below the V_{th} of HVT, only the LVT device enters its conduction state. Moreover, the W_g of D-mode and LVT are all 5 μm, therefore they have almost the same resistance value. And the LVT holds experiences the same share of the voltage division, thereby producing an intermediate state output voltage. When V_{in} further increases beyond the V_{th} of HVT, all transistors conduct. The W_g of the HVT is 50 μm. Therefore compared to D-mode, it has a lower resistance value and experiences a low share of the voltage division. This parallel conduction of two E-mode further reduces the total resistance, enabling a lower output voltage. Fig. 6(c) demonstrated the ternary logic output characteristics, exhibiting a V_{OH} of 6V and a V_{OL} of 0.12 V. The V_{IL1}, V_{IH1}, V_{IL2}, and V_{IH2} voltage levels, extracted from the voltage unit gain points ($dV_{out}/dV_{in} = -1$) are 1.16 V, 1.7 V, 2.02 V, and 2.5 V, respectively. Crucially, when V_{in} is greater than the V_{th} of LVT (1.16V) and less than the V_{th} of HVT (2.02V), a distinct 0.3V-wide input voltage plateau spanning $1.7V < V_{in} < 2.02$ V maintains a stable intermediate output level of 3V, which resides between the high and low logic states as the third state.

Fig. 6(d, e) represented the schematic diagram and optical macroscope of the ternary NAND, respectively. The W_g of D-mode, LVT, and HVT are 6 μm, 18 μm, and 60 μm, respectively. When three LVTs are turned on, their combined equivalent resistance becomes comparable to that of D-mode device. This results in an equivalent voltage division, thereby producing an intermediate output voltage level. When the HVT is turned on, its resistance is significantly lower than that of the D-mode. Consequently, it obtains a negligible portion of the voltage, resulting in a low-level output. As illustrated in Fig. 6(f), the output voltage descends from 6V to 3V and subsequently to 0V. The circuit maintains a high-level output at 6V when any input is at the low level. Conversely, when the minimum input is at 2.8V, the output is at the middle level of 3V. Under conditions where all inputs simultaneously attain the high level, the output voltage drops to the low-level state of 0V, thereby achieving three levels of output voltage and the circuit exhibits the correct output corresponding to each variation in input logic.

4. Conclusion

High performance GaN binary digital components were implemented by an argon-based NBE method, including inverter, AND, OR, NAND, and NOR. Inverter with high logic swing voltage (99.7%), balanced noise margin, and low transition period was achieved. AND, OR, NAND, and NOR digital gates were characterized showing excellent logic voltage swing and had a nanosecond level short response time. These digital components maintain reliable operation at elevated supply voltages up to V_{DD} of 8 V. Preliminary feasibility of implementing multi-value logic devices was verified by integrating devices with different threshold voltages. When $1.7V < V_{in} < 2.02V$, a 0.3V wide input voltage plateau is generated. At this point, the output voltage is 3V, between high and low levels, serving as the third logic state. These results highlight that NBE gate recessing offers a promising approach for the fabrication of high-performance normally-off GaN MOSHEMTs to be used in digital applications and show the enormous potential in

monolithic integration of multi-Vth devices to be used in power applications.

CRediT authorship contribution statement

Yudong Li: Writing – review & editing, Writing – original draft, Visualization, Methodology, Investigation, Data curation. **Han Gao:** Writing – original draft, Visualization, Methodology, Investigation, Data curation. **Xuanling Zhou:** Writing – review & editing, Methodology, Investigation. **Xinbo Zou:** Writing – review & editing, Supervision, Resources, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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